

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (cancelled)

Claim 2. (currently amended) A system comprising:

a memory, wherein the memory includes a plurality of logical memory devices; and
a network switch coupled to the memory, wherein the switch is configured ~~adaptable~~
to sequentially write a first portion of received packet data to a first of the plurality of logical memory devices and to write a second portion of the packet data to a second of the plurality of logical memory devices and to write a third portion of the packet data to a third of the plurality of logical memory devices.

Claim 3. (previously presented) The system of claim 2 wherein the network switch comprises a memory controller.

Claim 4. (original) The system of claim 3 wherein the memory controller comprises:
a first memory controller component coupled to the first logical memory device; and
a second memory controller component coupled to the second logical memory device.

Claim 5. (original) The system of claim 4 wherein the first memory controller component and the second memory controller component access the corresponding logical memory devices via a shared address line.

Claim 6. (previously presented) The system of claim 2 wherein the first, second and third of the plurality of logical memory devices comprise synchronous dynamic random access memories (SDRAMs).

Claim 7. (previously presented) The system of claim 2 wherein the first of the plurality of logical memory devices comprises a synchronous static random access memories (SSRAMs) and the second and third of the plurality of logical memory devices comprise synchronous dynamic random access memories (SDRAMs).

Claim 8. (currently amended) The system of claim 3 wherein the memory controller maintains a record identifying a logical memory device ~~of the last~~ of the plurality of logical memory devices that was last written to.

Claim 9. (original) The system of claim 3 wherein the network switch further comprises:
 a receiver coupled to the memory controller;
 a transmitter coupled to the memory controller;
 address resolution logic coupled to the memory controller; and
 packet queuing control coupled to the memory controller, the receiver, the transmitter and the address resolution logic.

Claim 10. (previously presented) The system of claim 9 wherein the network switch further comprises a media access controller (MAC) coupled to the receiver, wherein the MAC receives packet data via a plurality of ports coupled to the receiver.

Claim 11. (cancelled)

Claim 12. (currently amended) A network switch comprising:
 a first media access controller (MAC) coupled to a plurality of ports;
 a receiver coupled to the first MAC; and
 a memory controller coupled to the receiver, wherein the memory controller is configured ~~adaptable~~ to write a first portion of a first data packet received from a first of the plurality of ports to a first logical memory device and write a second portion of the first data packet received from the first port to a second logical memory device and to write a third

portion of the first data packet received from the first port to a third logical memory device during a single memory write access.

Claim 13. (currently amended) The system of claim 12 wherein the memory controller is configured ~~adaptable~~ to write a first portion of a second data packet received from the first port to a fourth logical memory device and write a second portion of the second data packet received from the first port to a fifth logical memory device.

Claim 14. (currently amended) The system of claim 12 wherein the memory controller is configured ~~adaptable~~ to write a first portion of a first data packet received from a second of the plurality of ports to the first logical memory device and write a second portion of the first data packet received from the second port to the second logical memory device.

Claim 15. (previously presented) The system of claim 12 wherein the memory controller comprises:

- a first memory controller component coupled to the first logical memory device; and
- a second memory controller component coupled to the second logical memory device.

Claim 16. (original) The system of claim 15 wherein the first memory controller component and the second memory controller component access the corresponding logical memory devices via a shared address line.

Claim 17. (original) The system of claim 12 wherein the first, second and third logical memory devices comprise synchronous dynamic random access memories (SDRAMs).

Claim 18. (currently amended) The system of claim 12 wherein the first logical memory device comprises a synchronous static random access memory ~~memories~~ (SSRAMs) and the second and third logical memory devices comprise synchronous dynamic random access memories (SDRAMs).

Claim 19. (cancelled)

Claim 20. (currently amended) A method comprising:

receiving a first data packet at a network switch; and

performing a first memory write access wherein

~~writing~~ a first portion of the first data packet is written to a first logical memory device coupled to the network switch; ~~and~~

~~writing~~ a second portion of the first data packet is written to a second logical memory device coupled to the network switch and

~~writing~~ a third portion of the first data packet is written to a third logical memory device coupled to the network switch.

Claim 21. (previously presented) The method of claim 20 further comprising:

receiving a second data packet at the network switch;

writing a first portion of the second data packet to the first logical memory device; and

writing a second portion of the second data packet to the second logical memory device.

Claim 22. (currently amended) The method of claim 20 further comprising determining at the network switch the ~~last~~ logical memory device to which a portion of the first data packet was last written.

Claim 23. (currently amended) The method of claim 20 further comprising:

determining whether the size of a third portion of the data packet is less than a predetermined value; and

if so, writing the third portion of the data packet to both banks of the a third logical memory device.

Claim 24. (currently amended) The method of claim 23 further comprising:

determining whether the size of the a third portion of the data packet is less than a predetermined value; and

if not, writing a first sub-portion of the third portion of the data packet to a first bank of a third logical memory device and writing a second sub-portion of the third portion of the data packet to a second bank of the third logical memory device.

Claim 25. (new) A method of switching packets within a network comprising:

receiving a first data packet from a first port;

parsing the first data packet into a plurality of first data packet portions;

writing a first data packet portion of the plurality of first data packet portions to a first logical memory device of a plurality of logical memory devices;

writing a second data packet portion of the plurality of first data packet portions to a second logical memory device of the plurality of logical memory devices;

receiving a second data packet from the first port;

parsing the second data packet into a plurality of second data packet portions;

determining which of the plurality of logical memory devices was the last of the plurality of memory devices to which one of the plurality of first data packet portions was written; and

writing a first data packet portion of the plurality of second data packet portions to one of the plurality of logical memory devices other than the last of the plurality of memory devices.

Claim 26. (new) The method of claim 25, wherein the step of writing a first data packet portion of the plurality of second data packet portions comprises:

writing the first data packet portion of the plurality of second data packet portions to the first logical memory device of the plurality of logical memory devices.

Claim 27. (new) The method of claim 26, further comprising:

writing a second data packet portion of the plurality of second data packet portions to one of the plurality of logical memory devices other than the last of the plurality of memory devices.

Claim 28. (new) The method of claim 27, wherein:

the method further comprises the step of writing a third data packet portion of the plurality of first data packet portions to a third logical memory device of the plurality of logical memory devices; and

the step of writing a second data packet portion of the plurality of second data packet portions to one of the plurality of logical memory devices other than the last of the plurality of memory devices comprises the step of writing the second data packet portion of the plurality of second data packet portions to a fourth logical memory device of the plurality of logical memory devices.